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(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)and (distribut\$ near4 processor\$) (non-volatile\$ or rom\$ or bios\$) and (request\$ near9 processor\$)	0

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<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
	<i>DB=TDBD; PLUR=YES; OP=ADJ</i>		
<u>L21</u>	(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)and (distribut\$ near4 processor\$) (non-volatile\$ or rom\$ or bios\$ ) and (request\$ near9 processor\$)	0	<u>L21</u>
	<i>DB=DWPI; PLUR=YES; OP=ADJ</i>		
<u>L20</u>	(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)and (distribut\$ near4 processor\$) (non-volatile\$ or rom\$ or bios\$ ) and (request\$ near9 processor\$)	0	<u>L20</u>
	<i>DB=JPAB; PLUR=YES; OP=ADJ</i>		
<u>L19</u>	(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)and (distribut\$ near4 processor\$) (non-volatile\$ or rom\$ or bios\$ ) and (request\$ near9 processor\$)	0	<u>L19</u>
	<i>DB=EPAB; PLUR=YES; OP=ADJ</i>		

<u>L18</u>	(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)and (distribut\$ near4 processor\$) (non-volatile\$ or rom\$ or bios\$ ) and (request\$ near9 processor\$)	0	<u>L18</u>
	<i>DB=USOC; PLUR=YES; OP=ADJ</i>		
<u>L17</u>	(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)and (distribut\$ near4 processor\$) (non-volatile\$ or rom\$ or bios\$ ) and (request\$ near9 processor\$)	0	<u>L17</u>
	<i>DB=PGPB; PLUR=YES; OP=ADJ</i>		
<u>L16</u>	(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)and (distribut\$ near4 processor\$) (non-volatile\$ or rom\$ or bios\$ ) and (request\$ near9 processor\$)	0	<u>L16</u>
	<i>DB=USPT; PLUR=YES; OP=ADJ</i>		
<u>L15</u>	714/13.ccls.	263	<u>L15</u>
<u>L14</u>	711/5.ccls.	758	<u>L14</u>
<u>L13</u>	709/220,221,201.ccls.	2108	<u>L13</u>
<u>L12</u>	L9 and l4	10	<u>L12</u>
<u>L11</u>	L9 and l6	4	<u>L11</u>
<u>L10</u>	L9 and l8	1	<u>L10</u>
<u>L9</u>	717/149,172,177,178.ccls.	349	<u>L9</u>
<u>L8</u>	L7 and stor\$	162	<u>L8</u>
<u>L7</u>	L5 and (request\$ near9 processor\$)	162	<u>L7</u>
<u>L6</u>	L5 and control\$	280	<u>L6</u>
<u>L5</u>	L4 and (Manag\$ near4 processor\$)	282	<u>L5</u>
<u>L4</u>	L2 and (non-volatile\$ or rom\$ or bios\$ )	1067	<u>L4</u>
<u>L3</u>	L2 and (on-volatile\$ or rom\$ or bios\$ )	951	<u>L3</u>
<u>L2</u>	L1 and (distribut\$ near4 processor\$)	2948	<u>L2</u>
<u>L1</u>	(plural\$ or multi\$ or number\$) near4 processor\$ and memory and (software\$ or component\$ or module\$ or entity\$)	31796	<u>L1</u>

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### Search Results -

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L1 and upload\$	1

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<u>L11</u>	l1 and upload\$	1	<u>L11</u>
<u>L10</u>	l1 and cop\$	1	<u>L10</u>
<u>L9</u>	l1 and (reposit\$ or warehouse\$) near4 (mainframe\$ or central\$)	1	<u>L9</u>
<u>L8</u>	l1 and (modif\$ or unmodif\$) near5 reposit\$	1	<u>L8</u>
<u>L7</u>	l1 and (verif\$ or check\$)	1	<u>L7</u>
<u>L6</u>	l1 and (design\$ or desig\$ or re-design\$ or replac\$ or chang\$ or modif\$ or alternat\$) near9 (reposit\$ or warehouse\$ or database\$)	1	<u>L6</u>
<u>L5</u>	l1 and (start\$ or boot\$ or reset\$ or set\$ or initiat\$ or operating system\$ or o/s)	1	<u>L5</u>
<u>L4</u>	L3 and (initiat\$ or boot\$ or start\$)	0	<u>L4</u>
<u>L3</u>	l1 and (warehouse\$ or local\$ or primary\$)	1	<u>L3</u>
<u>L2</u>	L1 and bank\$	0	<u>L2</u>
<u>L1</u>	5495610.pn.	1	<u>L1</u>

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**1 [CRL: high-performance all-software distributed shared memory](#)**

K. L. Johnson, M. F. Kaashoek, D. A. Wallach

 December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles**, Volume 29 Issue 5
Full text available: [pdf\(2.02 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)
**2 [Towards transparent and efficient software distributed shared memory](#)**

Daniel J. Scales, Kourosh Gharachorloo

 October 1997 **ACM SIGOPS Operating Systems Review , Proceedings of the sixteenth ACM symposium on Operating systems principles**, Volume 31 Issue 5
Full text available: [pdf\(2.34 MB\)](#)Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)
**3 [Algorithms for scalable synchronization on shared-memory multiprocessors](#)**

John M. Mellor-Crummey, Michael L. Scott

 February 1991 **ACM Transactions on Computer Systems (TOCS)**, Volume 9 Issue 1
Full text available: [pdf\(3.07 MB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Busy-wait techniques are heavily used for mutual exclusion and barrier synchronization in shared-memory parallel programs. Unfortunately, typical implementations of busy-waiting tend to produce large amounts of memory and interconnect contention, introducing performance bottlenecks that become markedly more pronounced as applications scale. We argue that this problem is not fundamental, and that one can in fact construct busy-wait synchronization algorithms that induce no memory or interc ...

**4 [Removing the overhead from software-based shared memory](#)**

Zoran Radović, Erik Hagersten

 November 2001 **Proceedings of the 2001 ACM/IEEE conference on Supercomputing (CDROM)**
Full text available: [pdf\(237.99 KB\)](#)Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The implementation presented in this paper---DSZOOM-WF---is a sequentially consistent, fine-grained distributed software-based shared memory. It demonstrates a protocol-

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